

DESIGN NOTES

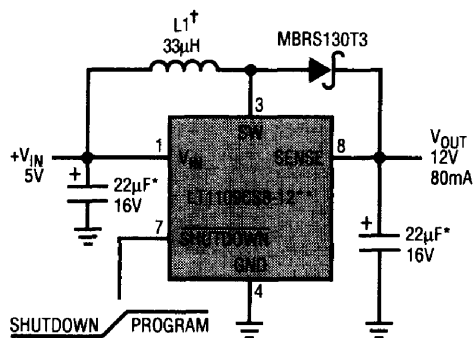
A Simple, Surface Mount Flash Memory Vpp Generator – Design Note 58

Steve Pietkiewicz
Jim Williams

“Flash” type memories add electrical chip-erase and reprogramming to established EPROM technology. These features make them a cost effective and reliable alternative for updatable non-volatile memory. Utilizing the electrical program-erase capability requires linear circuitry techniques. Intel flash memory, built on the ETOX™ process, specifies programming operation with 12V amplitude pulses. These “Vpp” amplitudes must fall within tight tolerances, and excursions beyond 14.0V will damage the device.

Providing the Vpp pulse requires generating and controlling high voltages within the tightly specified limits. Figure 1’s circuit does this. When the Vpp command pulse goes high (trace A, Figure 2) the LT1109 switching regulator drives L1, producing high voltage. DC feedback occurs via the regulator’s sense pin. The result is a smoothly rising Vpp pulse (trace B) which settles to the required value. Trace C, a time and amplitude expanded version of trace B, details the desired settling to 12V. Artifacts of the switching regulator’s action are discernible, although no overshoot or poor dynamics are displayed.

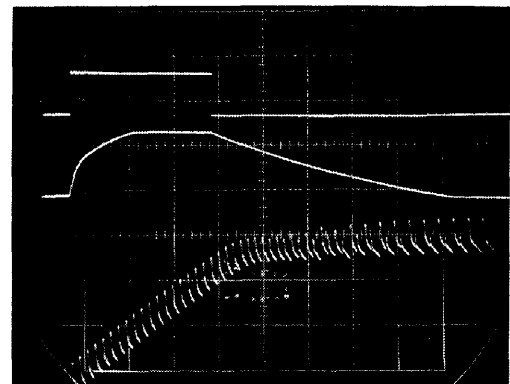
ETOX is a trademark of Intel Corporation.



† L1 = SUMIDA CD54-330N (708-956-0666)
* HILTON CSTDD226M016TC (813-371-2600)
** USE LT1109A FOR 120mA OUTPUT (CONSULT LTC FACTORY)

DN58 • TA02

TRACE A = 5V/DIV
TRACE B = 5V/DIV
TRACE C = 0.1V/DIV (OUTPUT)



A & B HORIZ = 1 ms/DIV
C HORIZ = 50µs/DIV

DN58 • TA03

Figure 1. All Surface Mount Flash Memory Vpp Generator

Figure 2. Waveforms for the Flash Memory Pulser Show No Overshoot

This circuit is well suited for providing V_{pp} power to flash memory. All associated components, including the inductor, are surface mount devices. As such, the complete circuit occupies very little space (see Figure 3). In the shutdown mode the circuit pulls only $300\mu A$. Output voltage goes to V_{CC} minus a diode drop when the converter is in shutdown mode. This is an acceptable and specified condition for flash memories and does not harm the memory. A $0V$ output is possible by placing a $5.6V$ Zener diode in series with the output rectifier (Figure 4A). An alternative configuration, suggested by J. Dutra of LTC, AC couples the output to achieve a $0V$ output (Figure 4B). Both of these methods add component count, decrease efficiency and slightly limit available output current. They are unnecessary unless the user desires a $0V$ output on the V_{pp} line.

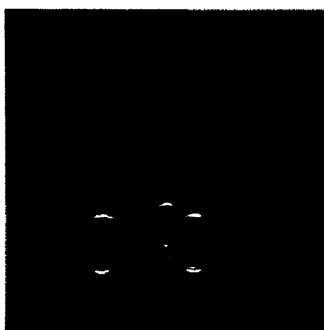


Figure 3. Simple Flash Memory Pulser Uses All Surface Mount Components

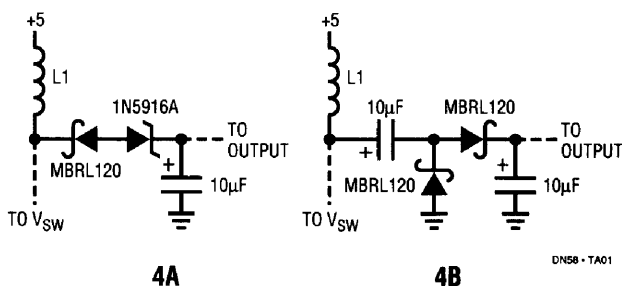


Figure 4. Two Arrangements for Obtaining a 0V Output

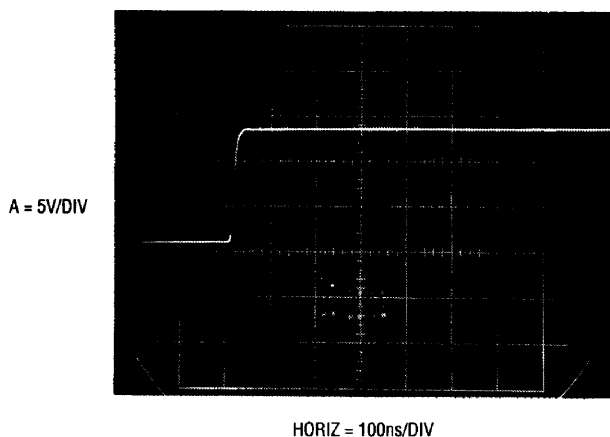


Figure 5. An "Ideal" Flash EPROM V_{pp} Pulse

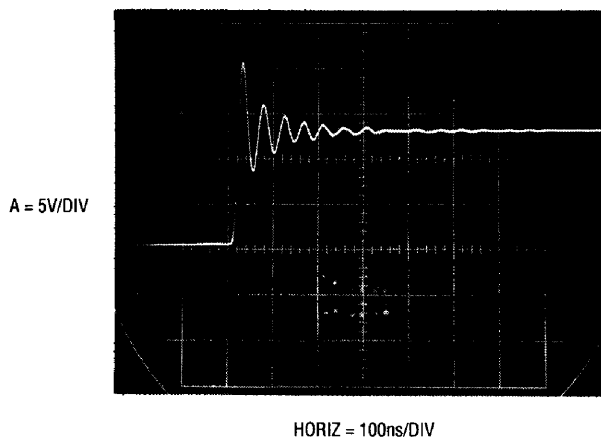


Figure 6. Rings at Destructive Voltages After a PC Trace Run

For literature on our DC-DC Converters, call (800) 637-5545. For applications help, call (408) 432-1900, Ext. 456